A 4μW, ADPLL-Based Implantable Amperometric Biosensor in 65nm CMOS

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Abstract

This paper presents a fully implantable, wirelessly powered subcutaneous amperometric biosensor. We propose a novel ultra-low power all-digital phase-locked loop (ADPLL) based potentiostat architecture for electrochemical sensing. The system is wirelessly powered by near-field RF coupling of an on-chip antenna to an external coil at 915 MHz. Bi-directional wireless telemetry supports data transmission from the sensor to the external reader (uplink) via backscattering, and reconfiguration of the sensor chip over the RF downlink. The 1.2×1.2 mm^2 prototype is fabricated in TSMC 65nm CMOS process. The potentiostat achieves a 100pA sensitivity over a full scale current range of 0-350nA. The total power consumption of the system is 4μW.

Keywords: Potentiostat, Wireless Power Transfer, All-Digital Phase Locked Loop, Implantable Medical Device.

Introduction

Miniaturization of implantable biosensors for continuous, *in-vivo* monitoring of clinically relevant analytes is an important step toward viability of such devices. While wireless power delivery via on-chip antennas promises miniaturization and realization of minimally invasive devices, it can only support low levels of power consumption. This is due to the significant tissue absorption at high frequencies, small size of the chip and quality factor of on-chip inductors [1]. Therefore, reducing the power consumption of the sensor while maintaining high sensitivity and dynamic range is crucial.

In this work we propose an ultra-low power potentiostat that achieves sensitivity and meets the dynamic range requirements of *in-vivo* amperometric sensing. We present a 1.2×1.2mm^2 fully implantable device with integrated electrodes, wireless power harvesting and data communication, Fig.1. The electrodes are post-processed and functionalized, and performance of the implant is verified via *in-vitro* measurements in hydrogen peroxide. The system consumes 4μW of power, and can accurately detect input currents ranging from 100pA to 350nA with a sensitivity of 100pA over the full range.

Potentiostat Architecture

Potentiostats find use in a wide range of biomedical applications. However, a number of key design considerations are necessary for the potentiostat to produce reliable data. In many applications, a small Faradaic current must be measured over a large DC offset, thus necessitating high sensitivity and high dynamic range – typically from less than 1nA to more than 300nA. Additionally, while it is highly desirable to reduce the voltage levels of the chip for energy saving, very low voltage levels are prohibitive as the redox potentials of biologically relevant analytes are typically between 0.4-0.7V.

There are two common architectures for measuring the output current of a potentiostat. The first is to convert the current to a voltage using a transimpedance amplifier [2]. This architecture suffers from a direct trade-off between dynamic range and supply voltage, since the shunt resistor reduces the headroom for the potentiostat redox potential. The second approach [3] involves converting the current-to-frequency using a relaxation oscillator, where the period of oscillation is set by the integration of the current into a capacitor. In this case, there is a trade-off between dynamic range and power consumption; large input signals translate to high frequency oscillations, thus more power consumption.

We propose a novel low power ADPLL-based architecture (Fig. 2) to obtain high dynamic range and sensitivity. The architecture employs a current-to-frequency converter with the modification that it maintains a constant oscillation frequency by dynamically adjusting the integration capacitor, a digitally-tunable capacitor (DTC), as the input signal changes. Fig. 2 shows the architecture of the ADPLL. The DCO is a relaxation oscillator whose frequency depends on the input current and the digital code supplied to the 12-bit DTC. This capacitor has an LSB of 10fF, set by the parasitic capacitance of the switches and the analog front-end current noise floor of 70pA. The DCO output is phase/frequency locked to a 32kHz reference clock. Both signals are fed to the input of the phase-frequency detector (PFD). The PFD output pulse width is proportional to the phase offset between DCO and reference clock. This pulse width is digitized at the time-to-digital converter (TDC) and then filtered through the PI digital loop filter (DLF). The output of the filter is fed back to the DTC to complete the loop. The DTC value is therefore proportional to the input current and can be read out immediately. Apart from the DCO, the entire ADPLL is implemented digitally using standard cells. This allows for reconfigurability, and the chip can be programmed to operate over various input current ranges.

Fig. 4 shows the details of potentiostat measurements and characterizations. The capacitance of the DTC was measured by supplying a DC current and measuring the DCO frequency at each of the 4096 digital code values of the DTC. A best-fit line shows 11.5fF per digital code, which agrees with our simulations. The large parasitic capacitance of 18.2pF is an artifact of the characterization test structure and current source output capacitance in the test setup. The current-measuring capability of the loop was tested from 0–350nA. Our measurements also verified an average offset current of 9.3 pA.

Power and Data Telemetry

The system is powered up wirelessly by near-field RF, and can communicate bi-directionally. A two-turn on-chip coil is used for RF power transfer and data telemetry. It is designed to maximize the RF power transfer efficiency at 915 MHz when the external reader (1.5cm diameter) is located 1cm away. The thick top copper metal layer is used for the on-chip coil to maximize the quality factor (Q~20). A 2pF MIM capacitor resonates with the on-chip coil at 915 MHz.

A 3-stage self-synchronous full wave rectifier ramps up the

rectified signal to a sufficiently high voltage of 1.2V (Fig. 3). A 1nF MOS capacitor at the output of the rectifier reduces ripple. The simulated maximum conversion efficiency of the rectifier is 60%. The LDO, shown in Fig. 3, generates a stable 1V supply for a load current range of 200pA-5µA. A 500pF MOS output capacitor ensures LDO stability, high frequency power supply rejection, and provides high transient currents. The measured efficiency of the LDO was 75%. PWM-ASK modulation is used to reconfigure the sensor. Once the sensor finishes recording, the digitized bits are sent to the external reader by RF backscattering (Fig. 5).

In-vitro Experimental Results

The chip prototype was fabricated in a 65nm CMOS technology, Fig.6. The three electrodes, working (WE), counter (CE), and reference (RE), were fabricated by a metal liftoff photolithography process on top of the original aluminum electrodes.

125nm of Pt was sputtered to serve as an inert electrode surface that would not affect the measured redox reactions. The functionality of the sensor was validated in the clinically relevant concentration ranges (0-0.8mM) of hydrogen peroxide commonly seen in clinically relevant oxidase enzyme-based biosensors, using amperometry with a 0.4V potential between WE and RE (Fig.4). Table 1 summarizes the performance of the system and compares to the state-of-the-art.

References

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[3] Nazari et al., ***TBioCAS***, June 2013.
[4] Mamum et al., ***TBioCAS***, Aug. 2016.
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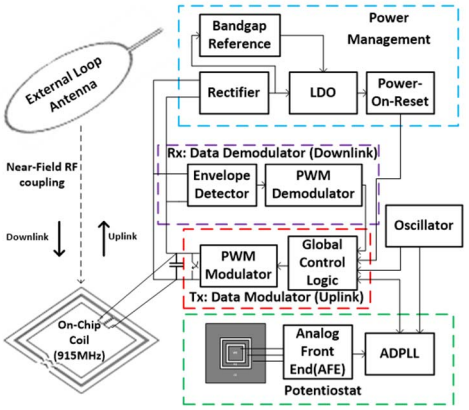

Fig.1 Block diagram of the implantable potentiostat system

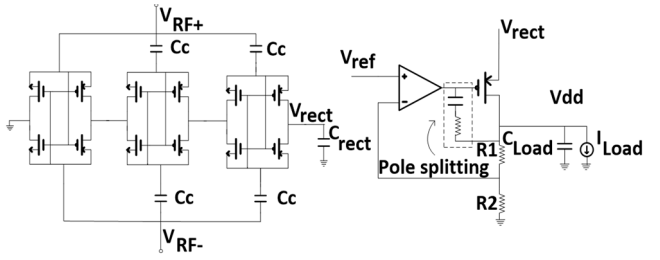

Fig.3 Circuit topologies of rectifier and LDO

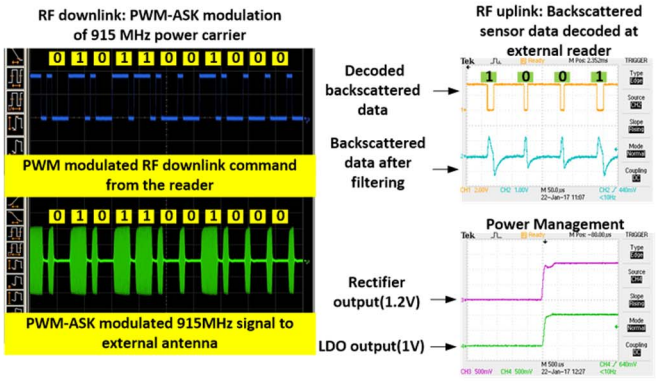

Fig.5 Power management and data telemetry measurements

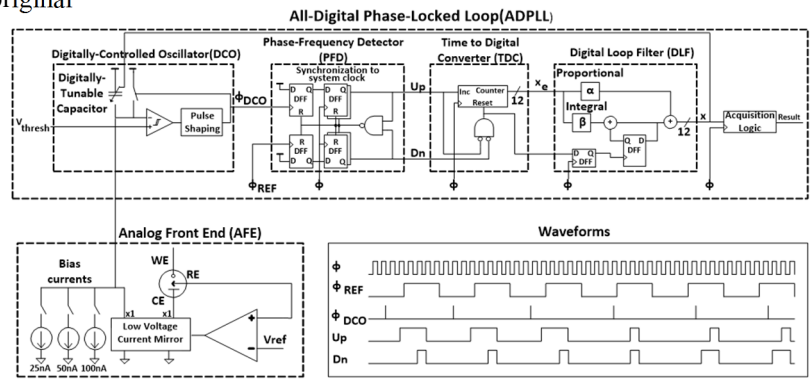

Fig.2 Architecture of the ADPLL based potentiostat

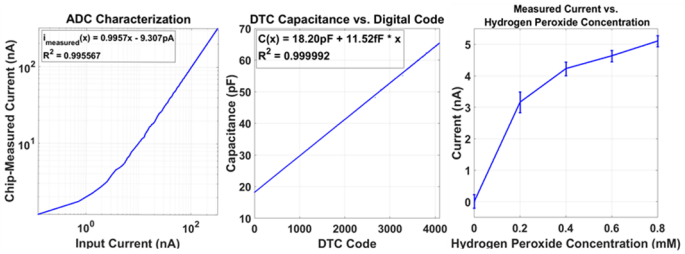

Fig.4 *In-vitro* hydrogen peroxide potentiostat measurements and characterization

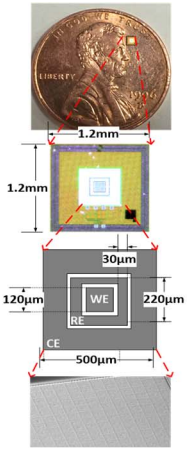

Fig.6 Die diagram

Table 1

Performance Metric	This work	[4]	[5]	[6]
Potentiostat Architecture	CM+ItF+ADPLL	CM+TIA+VCO	TIA+ADC	CM+Ring Osc.
Power	4µW	71.7µW	6µW	3µW
Voltage	1V	1.8V	1.2V	1.2V
System Area	1.2mm×1.2mm	Not Reported	1.4mm×1.4mm	1cm diameter*
Measurement Range	350nA	7µA	500nA	150nA
Measurement Sensitivity	100pA	500nA	2nA**	2nA
Wireless	Yes	No	Yes	Yes
Integrated Electrodes	Yes	No	Yes	Yes
Electrode Size	0.5mm×0.5mm	0.3mm×0.3mm	0.5mm×0.5mm	1.6mm×1.9mm
Electrode Material	Pt	Carbon Nanofiber	Pt,Ag/AgCl	Ti/Pd/Pt
Process	65nm	180nm	180nm	130nm

Architecture shorthands: CM = current mirror; ItF = current-to-frequency convertor; TIA = transimpedance amplification
*Including off-chip antenna
**Maximum sensitivity with a full scale range of 500nA